CLAIMS

What is claimed is:

1. A method of improving the efficiency of a synchronous mirror delay circuit comprising:

providing a clock input signal (CIN), an inverted clock input signal (CIN')and a clock delay signal (CDLY);

detecting a plurality of phases of CIN and CDLY based on timing conditions associated with CIN and CDLY; and

selectively inputting CIN or CIN' into a synchronous mirror delay (SMD) based on the phase of CIN and CDLY to reduce a number of required delay stages in the SMD.

2. The method of claim 1 wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}) and wherein the selectively inputting step includes inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ to reduces the number of required delay stages in the SMD.

3. The method of claim 2 wherein the number of delay stages in the SMD is reduced substantially in half.

4. The method of claim 2 wherein the SMD has a plurality of delay lines and wherein the number of delay stages in at least one of the SMD delay lines is reduced substantially to 59 from 128.

5. A method of improving the efficiency of a synchronous mirror delay circuit comprising the steps of:

providing a clock input signal (CIN), an inverted clock input signal (CIN') and clock delay signal (CDLY), each signal having timing characteristics;

interposing a phase detector and selection system between an external clock signal and a synchronous mirror delay circuit;

determining which of a number of phases the signals are in based on the timing characteristics; and

selectively directing the signals based upon the phase of the signals.

6. The method of claim 5 wherein the selectively directing step includes selectively directing CIN or CIN' to the synchronous mirror delay based upon the timing characteristics of CIN and CDLY.

7. The method of claim 5 wherein the selectively directing step includes bypassing CIN or CIN' from the synchronous mirror delay based upon the timing characteristics of CIN and CDLY.

8. The method of claim 5 further including defining the timing characteristics as a period of CIN as t_{ck} and defining a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein the determining steps includes determining that the phases include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$;

a fourth phase when $t_{mdl} = t_{ck}/2$.

9. A method of reducing a number of effective delay stages in a synchronous mirror delay (SMD), the method comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN') and a clock delay signal (CDLY) having timing characteristics;

differentiating, with a phase detector, a plurality of phases based upon the timing characteristics of CIN and CDLY; and

selecting, based on the phases, one of CIN and CIN' to be input into a synchronous mirror delay, thereby reducing the effective delay stages in the SMD.

10. A method of reducing a number of effective delay stages in a synchronous mirror delay (SMD), the method comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN') and a clock delay signal (CDLY) having timing characteristics;

determining a plurality of phases based upon the timing characteristics of CIN and CDLY;

for at least one phase, directing CIN' into the synchronous mirror delay such that a reduced number of delay stages are achieved.

11. The method of claim 10 wherein the timing characteristics define a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein the directing step occurs when $t_{mdl} < t_{ck}/2$.

12. The method of claim 11 further including the steps of:

multiplexing an input with an input selection multiplexor to select whether to direct the CIN or CIN' into the SMD, based on the phase determined in the determining step; and

multiplexing, with an output selection multiplexor, an output of the input selection multiplexor with an SMD output, the output selection multiplexor selecting whether to output, based on the phase determined in the determining step, the SMD output or CIN bypassing the SMD, as an input to a clock tree to generate an internal clock signal.

13. A memory device comprising:

a synchronous mirror delay (SMD) circuit; and

a phase detector connected to the SMD, the phase detector receiving a clock input signal and a clock delay signal, the clock input signal (CIN) and the clock delay signal (CDLY) each having timing characteristics, the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions of the clock input signal and the clock delay signal based on the timing characteristics, and wherein at least one of the conditions reduces a number of effective delay stages in the SMD.

14. The circuit of claim 13 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and

wherein a first phase is when $t_{mdl} > t_{ck}/2$;

wherein a second phase is when $t_{mdl} < t_{ck}/2$;

wherein a third phase is when $t_{mdl} = t_{ck}$; and

wherein a fourth phase is when $t_{mdl} = t_{ck}/2$.

15. The circuit of claim 14 wherein when $t_{mdl} < t_{ck}/2$ the number of effective delay stages in the SMD is comparable to when $t_{mdl} > t_{ck}/2$.

16. The circuit of claim 14 wherein the number of effective delay stages when $t_{mdl} < t_{ck}/2$ is reduced by substantially one-half.

17. The circuit of claim 14 wherein the number of effective delay stages when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

18. A synchronous mirror delay system comprising:

a synchronous mirror delay (SMD); and

a phase detector associated with the SMD, the phase detector receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and the CDLY each having timing characteristics, the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions based on the timing characteristics of CIN and CDLY, and wherein at least one of the conditions reduces the number of effective delay stages in the SMD;

wherein the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein the plurality of conditions include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$;

wherein the number of effective delay stages in the second phase is reduced; and

wherein in the third and fourth phases, CIN bypasses the SMD.

19. A synchronous mirror delay circuit for use with an external clock signal comprising:

an input buffer having an input connected to the external clock signal and an output connected to a clock input signal (CIN), an inverted clock input signal (CIN') and a clock delay signal (CDLY) each having timing characteristics;

a synchronous mirror delay (SMD) having a measurement delay line input for connection to a measurement delay line, a measurement delay line output connected to a variable delay line input for connection to a variable delay line, the variable delay line including a variable delay line output; and

a phase detector disposed between the input buffer and the synchronous mirror delay, the phase detector having a first input for receiving the CIN, a second input for receiving the CDLY, the phase detector generating one of a plurality of output signal combinations, each combination corresponding to a phase of the signals based on the timing characteristics, a CDLY SMD input connected to the measurement delay line input, and an SMD output connected to the variable delay line output, the circuit selectively inputting CIN or CIN' as a CIN SMD input based on the phase of the signals, and wherein at least one of the phases reduces a number of effective delay stages of the SMD.

20. The circuit of claim 19 wherein the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein when $t_{mdl} < t_{ck}/2$, CIN' is input into the SMD and when $t_{mdl} > t_{ck}/2$ CIN is input into the SMD.

21. The circuit of claim 20 wherein the number of effective delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced.

22. The circuit of claim 20 wherein the number of effective delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

23. A synchronous mirror delay system comprising:

a synchronous mirror delay (SMD); and

a phase detector in operational association with the SMD, the phase detector receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and the CDLY each having timing characteristics, the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions based on the timing characteristics, and wherein a number of effective delay stages of the SMD is reduced.

24. The system of claim 23 wherein under one condition the number of effective delay stages is reduced by substantially one-half .

25. The system of claim 23 wherein the timing characteristics defines a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein the plurality of conditions include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$; and

wherein in the second phase, the number of effective delay stages of the SMD is reduced.

26. A phase detection and selection circuit comprising:

a phase detector for receiving a clock input signal (CIN), an inverted clock input signal (CIN') and a clock delay signal (CDLY), each signal having timing conditions, and generating a plurality of output signal combinations, each combination based upon the timing conditions; and

logic associated with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals; and

wherein the phase detection and selection system selectively feeds CIN or CIN' into a synchronous mirror delay upon which plurality of output signal combinations is generated and wherein a number of effective delay stages is reduced.

27. The circuit of claim 26 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and wherein the phases include:

a first phase when $t_{mdl} > t_{ck}/2$; and

a second phase when $t_{mdl} < t_{ck}/2$; and

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$.

28. The circuit of claim 27 wherein the number of effective delay stages is reduced.

29. The circuit of claim 27 wherein number of effective delay stage is reduced substantially by one-half.

30. The circuit of claim 27 wherein the number of effective delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

31. A phase detection system for use with an external clock signal comprising:

a pair of registers, each register receiving a clock input signal (CIN) and a clock delay signal (CDLY), the registers including a pair of inputs and outputting a pair of outputs having one of a plurality of output signal combinations, each output signal combination representative of a condition based upon the timing characteristics of CIN and CDLY, the number of effective delay stages is reduced.

32. The system of claim 31 wherein the registers are D-type flip-flops.

33. The system of claim 31 wherein the phase detection system further includes:

an input selection multiplexor to select which of CIN and an inverted CIN (CIN') are to be inputted into the synchronous mirror delay; and

an output selection multiplexor connected to the input selection multiplexor and capable of receiving a synchronous mirror delay output from the SMD, the output selection multiplexor selecting whether to output the SMD output or CIN, where the output of the output selection multiplexor is used as an input to the clock tree to generate an internal clock signal.

34. A system comprising:

a processor;

a memory controller;

a plurality of memory devices;

a first bus interconnecting the processor and the memory controller;

a second bus interconnecting the memory controller and the memory devices;

each of the memory devices having:

a synchronous mirror delay (SMD) circuit;

a phase detector for receiving a clock input signal (CIN) and a clock delay signal (CDLY), each signal having timing conditions, and generating a plurality of output signal combinations, each combination corresponding to phases of the signals based upon the timing conditions; and

logic associated with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals; and

wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}) and wherein inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ reduces a number of delay stages in the SMD.

35. A synchronous dynamic random access memory (SDRAM) comprising:

a synchronous mirror delay (SMD); and

a phase detection system, the phase detection system further including:

a phase detector connected to the SMD, the phase detector receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and CDLY each having timing characteristics, the phase detector including a pair of registers, the registers including a pair of inputs and a pair of outputs, each of the outputs having a logical level, wherein the logical levels of the register outputs define a plurality of output signal combinations, each of the output signal combinations representative of a phase based upon the timing characteristics of the CIN and CDLY, and wherein a number of effective delay stages in the SMD is reduced;

an input selection multiplexor connected to a control to select whether to input CIN or an inverted CIN signal (CIN') into the SMD, or alternatively, bypass the SMD based on the logical levels of the outputs of the phase detector; and

an output selection multiplexor connected to the input selection multiplexor and the SMD and capable of receiving a SMD output from the SMD, the output selection multiplexor connected to a control to select whether to output one of the SMD output and an output of the input selection multiplexor, wherein the output of the output selection multiplexor is used as a clock tree input to generate an internal clock signal;

wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and

wherein the first phase is when $t_{mdl} > t_{ck}/2$; and

wherein the second phase is when is when $t_{mdl} < t_{ck}/2$; and

wherein the third phase is when $t_{mdl} = t_{ck}$; and

wherein the fourth phase is when $t_{mdl} = t_{ck}/2$.

36. The circuit of claim 35 wherein when $t_{mdl} < t_{ck}/2$ the number of effective delay stages in the SMD is comparable to when $t_{mdl} > t_{ck}/2$.

37. The circuit of claim 35 wherein a number of delay stages is reduced while maintaining a desired operating range.

38. The circuit of claim 35 wherein the lock period is substantially one clock period when $t_{mdl} < t_{ck}/2$.

39. A method of improving the efficiency of a delay-locked loop circuit comprising:

providing a clock input signal (CIN), an inverted clock input signal (CIN') and a clock feedback signal (CKFB);

detecting a plurality of phases of CIN and CKFB based on timing conditions associated with CIN and CKFB; and

selectively inputting CIN or CIN' into a delay-locked loop (DLL) based on the phase of CIN and CKFB to reduce a number of required delay stages in the DLL.

40. The method of claim 39 wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CKFB (t_e) and wherein the selectively inputting step includes inputting CIN into the DLL when $t_e > t_{ck}/2$ and inputting CIN' into the DLL when $t_e < t_{ck}/2$ to reduce the number of required delay stages in the DLL.

41. The method of claim 40 wherein the number of delay stages in the DLL is reduced substantially in half.

42. The method of claim 40 wherein the number of delay stages in the DLL is reduced from 128 to substantially 59.

43. A method of improving the efficiency of a delay-locked loop circuit comprising the steps of:

providing a clock input signal (CIN), an inverted clock input signal (CIN') and clock feedback signal (CKFB), each signal having timing characteristics;

interposing a phase detector and selection system between an external clock signal and a delay-locked loop circuit;

determining which of a number of phases the signals are in based on the timing characteristics; and

selectively directing the signals based upon the phase of the signals.

44. The method of claim 43 wherein the selectively directing step includes selectively directing CIN or CIN' to the delay-locked loop based upon the timing characteristics of CIN and CKFB.

45. The method of claim 43 wherein the selectively directing step includes directing CIN or CIN' to a clock tree driver based upon the timing characteristics of CIN and CKFB.

46. The method of claim 43 further including defining the timing characteristics as a period of CIN as t_{ck} and defining a period from a rising edge in CIN to a rising edge in CKFB as t_e, and wherein the determining steps includes determining that the phases include:

a first phase when $t_e > t_{ck}/2$;

a second phase when $t_e < t_{ck}/2$;

a third phase when $t_e = t_{ck}$;

a fourth phase when $t_e = t_{ck}/2$.

47. A method of reducing a number of effective delay stages in a delay-locked loop (DLL), the method comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN') and a clock feedback signal (CKFB) having timing characteristics;

differentiating, with a phase detector, a plurality of phases based upon the timing characteristics of CIN and CKFB; and

selecting, based on the phases, one of CIN and CIN' to be input into a delay-locked loop, thereby reducing the effective delay stages in the DLL.

48. A method of reducing a number of effective delay stages in a delay-locked loop (DLL), the method comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN') and a clock feedback signal (CKFB) having timing characteristics;

determining a plurality of phases based upon the timing characteristics of CIN and CKFB;

for at least one phase, directing CIN' into the delay-locked loop such that a reduced number of delay stages is achieved.

49. The method of claim 48 wherein the timing characteristics define a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CKFB as t_e, and wherein the directing step occurs when $t_e < t_{ck}/2$.

50. The method of claim 49 further including the steps of:

multiplexing an input with an input selection multiplexor to select whether to direct the CIN or CIN' into the DLL, based on the phase determined in the determining step.

51. A memory device comprising:

a delay-locked loop (DLL) circuit; and

a phase detector connected to the DLL, the phase detector receiving a clock input signal and a clock delay signal, the clock input signal (CIN) and the clock feedback signal (CKFB) each having timing characteristics, the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions of CIN and CKFB signal based on the timing characteristics, and wherein at least one of the conditions reduces a number of effective delay stages in the DLL .

52. The circuit of claim 51 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CKFB is defined as t_e; and

wherein a first phase is when $t_e > t_{ck}/2$;

wherein a second phase is when $t_e < t_{ck}/2$;

wherein a third phase is when $t_e = t_{ck}$; and

wherein a fourth phase is when $t_e = t_{ck}/2$.

53. The circuit of claim 52 wherein when $t_e < t_{ck}/2$ a reduced number of effective delay stages in the DLL is achieved.

54. The circuit of claim 52 wherein the number of effective delay stages in the DLL is reduced substantially in half.

55. The circuit of claim 52 wherein the number of effective delay stages in the DLL is substantially 59.

56. A delay-locked loop system comprising:

a delay-locked loop (DLL); and

a phase detector associated with the DLL, the phase detector receiving a clock input signal (CIN) and a clock feedback signal (CKFB), the CIN and the CKFB each having timing characteristics, the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions based on the timing characteristics of CIN and CKFB, and wherein at least one of the conditions reduces the number of effective delay stages in the DLL;

wherein the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CKFB as t_e, and wherein the plurality of conditions include:

a first phase when $t_e > t_{ck}/2$;

a second phase when $t_e < t_{ck}/2$;

a third phase when $t_e = t_{ck}$; and

a fourth phase when $t_e = t_{ck}/2$.

57. A delay-locked loop circuit for use with an external clock signal comprising:

an input buffer having an input connected to the external clock signal and an output connected to a clock input signal (CIN), an inverted clock input signal (CIN') and a clock feedback signal (CKFB) each having timing characteristics;

a delay-locked loop (DLL);

a phase detector disposed between the input buffer and the delay-locked loop, the phase detector having a first input for receiving the CIN, a second input for receiving the CKFB, the phase detector generating one of a plurality of output signal combinations, each combination corresponding to a phase of the signals based on the timing characteristic;

wherein the delay-locked loop includes a delay line input, a selection multiplexor connected to the delay line, a clock tree driver for receiving an output of the selection multiplexor, and a feedback loop for connecting CKFB to the phase the circuit selectively inputting CIN or CIN' as a DLL input based on the phase of the signals, and wherein in at least one of the phases a number of effective delay stages of the DLL is reduced.

58. The circuit of claim 57 wherein the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CKFB as t_e, and wherein when $t_e > t_{ck}/2$, CIN is input into the DLL, and when $t_e < t_{ck}/2$, CIN' is input into the DLL.

59. The circuit of claim 58 wherein the number of effective delay stages in the DLL is reduced substantially in half.

60. The circuit of claim 58 wherein the number of effective delay stages in the DLL is substantially 59.

61. A delay-locked loop system comprising:

a delay-locked loop (DLL); and

a phase detector in operational association with the DLL, the phase detector receiving a clock input signal (CIN) and a clock feedback signal (CKFB), the CIN and the CKFB each having timing characteristics, the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions based on the timing characteristics, and wherein at least one of the conditions reduces a number of effective delay stages of the DLL.

62. The system of claim 61 wherein the number of effective delay stages is reduced substantially in half.

63. The system of claim 61 wherein the timing characteristics defines a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CKFB as t_e, and wherein the plurality of conditions include:

a first phase when $t_e > t_{ck}/2$;

a second phase when $t_e < t_{ck}/2$;

a third phase when $t_e = t_{ck}$; and

a fourth phase when $t_e = t_{ck}/2$; and

wherein the number of effective delay stages in the DLL is reduced.

64. A phase detection and selection circuit comprising:

a phase detector for receiving a clock input signal (CIN) and a clock feedback signal (CKFB), each signal having timing conditions, and generating a plurality of output signal combinations, each combination based upon the timing conditions; and

logic associated with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals; and

wherein the phase detection and selection system selectively feeds CIN or CIN' into a delay-locked loop based upon which of a plurality of output signal combinations is generated and wherein a number of effective delay stages is reduced.

65. The circuit of claim 64 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CKFB is defined as t_e; and wherein the phases include:

a first phase when $t_e > t_{ck}/2$; and

a second phase when $t_e < t_{ck}/2$; and

a third phase when $t_e = t_{ck}$; and

a fourth phase when $t_e = t_{ck}/2$.

66. The circuit of claim 65 wherein the number of effective delay stages is reduced.

67. The circuit of claim 65 wherein the number of effective delay stages is reduced substantially in half.

68. The circuit of claim 65 wherein the number of delay stages in the DLL is substantially 59.

69. A phase detection system for use with an external clock signal comprising:

a pair of registers, each register receiving a clock input signal (CIN) and a clock feedback signal (CKFB), the registers including a pair of inputs and outputting a pair of outputs having one of a plurality of output signal combinations, each output signal combination representative of a condition based upon the timing characteristics of CIN and CKFB, wherein under at least one of the conditions a number of effective delay stages is reduced.

70. The system of claim 69 wherein the registers are D-type flip-flops.

71. The system of claim 69 wherein the phase detection system further includes:

an input selection multiplexor to select which of CIN and CIN' are to be inputted into the delay-locked loop; and

a phase detector output input into the input selection multiplexor to select the inputs of the input selection multiplexor; and

a control block to receive control signals from the phase detector and input control signals to a delay line.

72. A system comprising:

a processor;

a memory controller;

a plurality of memory devices;

a first bus interconnecting the processor and the memory controller;

a second bus interconnecting the memory controller and the memory devices;

each of the memory devices having:

a delay-locked loop (DLL) circuit;

a phase detector for receiving a clock input signal (CIN) and a clock delay signal (CKFB), each signal having timing conditions, and generating a plurality of output signal combinations, each combination corresponding to phases of the signals based upon the timing conditions; and

logic associated with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals; and

wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CKFB (t_e) and wherein selectively inputting CIN into the delay-locked loop when $t_e < t_{ck}/2$ reduces a number of effective delay stages.

73. A synchronous dynamic random access memory (SDRAM) comprising:

a delay-locked loop (DLL); and

a phase detection system, the phase detection system further including:

a phase detector connected to the DLL, the phase detector receiving a clock input signal (CIN) and a clock feedback signal (CKFB), the CIN and CKFB each having timing characteristics, the phase detector including a pair of registers, the registers including a pair of inputs and a pair of outputs, each of the outputs having a logical level, wherein the logical levels of the register outputs define a plurality of output signal combinations, each of the output signal

combinations representative of a phase based upon the timing characteristics of the CIN and CKFB, and wherein at least one of the phases reduces a lock period of the CIN when input into the DLL to achieve locking with an external clock signal with respect to another phase;

an input selection multiplexor to select whether to input the CIN or CIN' into the DLL based on the logical levels of the outputs of the phase detector; and

wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CKFB is defined as t_e; and

wherein the first phase is when $t_e > t_{ck}/2$; and

wherein the second phase is when is when $t_e < t_{ck}/2$; and

wherein the third phase is when $t_e = t_{ck}$; and

wherein the fourth phase is when $t_e = t_{ck}/2$.

74. The circuit of claim 73 wherein when $t_e < t_{ck}/2$ the lock period to lock CIN to the external clock is reduced.

75. The circuit of claim 73 wherein when $t_e < t_{ck}/2$ the lock period to lock CIN to the external clock signal is reduced substantially in half with respect to a conventional delay locked loop.